WE CLAIM

1. A bridge circuit comprising:

a first interface circuit operable to receive data from a data source at a first data rate;

a second interface circuit operable to transmit said data to a data receiver at a second data rate;

a data coupling circuit comprising:

a synchronous coupling circuit operable to pass said data synchronously between said first interface circuit and said second interface circuit; and

an asynchronous coupling circuit operable to pass said data asynchronously between said first interface circuit and said second interface circuit, said bridge circuit further comprising

control logic responsive to a synchronous transfer request signal indicating that either said first data rate is an integer multiple of said second data rate or said second data rate is an integer multiple of said first data rate to cause data to be passed by said synchronous coupling circuit once any data within said asynchronous coupling circuit has been emptied.

2. The bridge circuit of claim 1, wherein said control logic is further operable in response to said synchronous transfer request signal to prevent said data source from supplying data to said first interface circuit until data within said asynchronous coupling circuit has been emptied.

3. The bridge circuit of claim 1, wherein said first interface circuit comprises a path operable to transmit a ready signal to said data source indicative of said asynchronous coupling circuit having capacity to receive further data.

4. The bridge circuit of claim 3, wherein said first interface circuit comprises an AMBA extensible interface and said ready signal is transmittable in association with one of its data channels.

5. The bridge circuit of claim 1, wherein said synchronous coupling circuit comprises a bus.

6. The bridge circuit of claim 5, wherein said control logic is operable in response to said synchronous transfer request signal to pass said data synchronously between said first interface circuit and said second interface circuit via said bus.

7. The bridge circuit of claim 1, wherein said control logic is responsive to said synchronous transfer request signal indicating that said first data rate and said second data rate are equal to cause data to be passed by said synchronous coupling circuit once any data within said asynchronous coupling circuit has been emptied.

8. The bridge circuit of claim 1, wherein said control logic is responsive to an asynchronous transfer request signal indicating that one of said first data rate and said second data rate will change to a value which is not an integer multiple of the other to cause data to be passed by said asynchronous coupling circuit before said change in said value occurs.

9. The bridge circuit of claim 8, wherein said asynchronous coupling circuit comprises a first-in first-out buffer operable to store said data from said data source at said first data rate and to read said data for transmission to said data receiver at said second data rate.

10. The bridge circuit of claim 9, wherein said control logic is operable in response to said asynchronous transfer request signal to pass said data asynchronously between said first interface circuit and said second interface circuit via said first-in first-out buffer.

11. In a bridge circuit comprising a first interface circuit operable to receive data from a data source at a first data rate, a second interface circuit operable to transmit said data to a data receiver at a second data rate, and a data coupling circuit comprising

a synchronous coupling circuit operable to pass said data synchronously between said first interface circuit and said second interface circuit and an asynchronous coupling circuit operable to pass said data asynchronously between said first interface circuit and said second interface circuit, a method of transferring data between said first interface circuit and said second interface circuit, said method comprising the steps of:

(a) providing a synchronous transfer request signal indicating that either said first data rate is an integer multiple of said second data rate or said second data rate is an integer multiple of said first data rate; and

(b) in response to receipt of said synchronous transfer request signal, causing data to be passed by said synchronous coupling circuit once any data within said asynchronous coupling circuit has been emptied.

12. The method of claim 11, further comprising the step of:

in response to said synchronous transfer request signal, preventing said data source from supplying data to said first interface circuit until data within said asynchronous coupling circuit has been emptied.

13. The method of claim 11, further comprising the step of:

providing a path operable to transmit a ready signal to said data source indicative of said asynchronous coupling circuit having capacity to receive further data.

14. The method of claim 13, wherein said first interface circuit comprises an AMBA extensible interface and said ready signal is transmittable in association with one of its data channels.

15. The method of claim 11, wherein said synchronous coupling circuit comprises a bus.

16. The method of claim 15, wherein said step (b) further comprises the step of:

in response to said synchronous transfer request signal, passing said data synchronously between said first interface circuit and said second interface circuit via said bus.

17. The method of claim 11, wherein said step (a) comprises the step of providing said synchronous transfer request signal indicating that said first data rate and said second data rate are equal.

18. The method of claim 11, further comprising the steps of:

providing an asynchronous transfer request signal indicating that one of said first data rate and said second data rate will change to a value which is not an integer multiple of the other; and

causing data to be passed by said asynchronous coupling circuit before said change in said value occurs.

19. The method of claim 18, wherein said asynchronous coupling circuit comprises a first-in first-out buffer operable to store said data from said data source at said first data rate and to read said data for transmission to said data receiver at said second data rate.

20. The method of claim 19, further comprising the step of:

in response to said asynchronous transfer request signal, passing said data asynchronously between said first interface circuit and said second interface circuit via said first-in first-out buffer.